REMARKS

With respect to the rejection to claim 1, lines 2-3, the claim has been clarified. The idea is that you add two columns to the compactor matrix for each scan chain that produces an unknown logic value at the same time as another scan chain produces an unknown logic value. It is believed that as clarified, the claim is clear.

With respect to the objection to claim 3, the maximum number of scan chains is determined in the method. Thus, the claim has been amended.

With respect to claim 5, the maximum compatibility class problem is a well known problem in digital circuit design. For example, see the website ClassShares.student.usp.ac.fj/EE22/2008%20(Current)/Lectures/IncomSpecifiedSys.pdf. This is apparently class notes for a course in which that problem is discussed. Thus, one skilled in the art would know what this is.

With respect to claim 8, the antecedent basis has been cleared up.

With respect to line 4 of claim 8, the claim has been amended.

With respect to claim 9, it is a product-by-process claim which is a well known type of claim. See M.P.E.P. § 2113.

With respect to claim 10, the claim has been amended to overcome the issue.

Claim 12 has been amended as suggested.

Claim 15 has been amended to overcome the antecedent problems.

With respect to claim 16, to handle any number of scan chains with unknown logic values means that the OR gates can handle 1, 2, 3, 4, or any number of scan chains that have unknown logic values. Reconsideration is requested. Lines 4 and 5 of claim 16 have been amended to clarify the issue raised.

The issue raised at the top of page 5 has been corrected.

The issue with respect to claims 17 and 18 has been addressed above.

Therefore, reconsideration is requested.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation